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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/007,082
Filing Date: December 6, 2001
Appellant(s): Linden Minnick, Patrick Connor

Erik Nordstrom (39,792)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed March 2, 2009 appealing from the Office action mailed February 1, 2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,905,874	JOHNSON	05-1999
7,065,762 B1	DUDA	06-2006
6,434,651	GENTRY, JR.	08-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 22, 20 and 29 are rejected under 35 U.S.C 103(a) as being unpatentable over Johnson, U.S. Patent 5,905,874 in view of Duda et al (hereinafter Duda), U.S. Patent Number 7,065,762 B1.

As per claim 1, Johnson in view of Duda discloses an apparatus comprising:

an input/output (I/O) device **210** [Figs. 2 & 3] being operative to:

receive a fragment of electronic data [Col 2, Lines 27-42] from a node on a network;

determine the characteristics of the fragment of electronic data; [Duda: col 5, L2] and

moderate one or more interrupts to a processor [Duda: col 5, L57 –col 6, L17] [Fig. 3] if the characteristics of the fragment of electronc data indicate that the fragment of electronic data is latency-sensitive data [Duda: col 5, L3-23] [Fig. 2B].

While Johnson discloses substantial features of the invention such as I/O device to receive packets and/or portions of packets (fragments) and initiating interrupts, as above, he does not explicitly disclose the additional features of determining the characteristics of the fragment of electronic data; and moderating one or more interrupts to a processor if the characteristics of the fragment of electronc data indicate that the fragment of electronic data is latency-sensitive data. The features are expressly disclosed by Duda in a related endeavor.

Duda discloses as his invention a scheduling mechanism that fairly allocates a resource to a number of schedulable elements of which some are *latency-sensitive*. The invention enforces long-term fairness to each element while allowing *latency-sensitive* elements to be preferably selected [Abstract] [col 2, L43-60]. In particular, Duda expressly discloses the additional recited features of determining the characteristics of the fragment of electronic data (e.g., "latency-sensitivity characteristics) [col 5, L2]; and moderating one or more interrupts to a processor [col 5, L57 –col 6, L17] [Fig. 3] if the characteristics of the fragment of electronc data indicate that the fragment of electronic data is latency-sensitive data (e.g., "the packet dispatch mechanism *253 examines the contents of the data packet*, and determines the level

service and output port(s) required by the data packet; determining if packet content is "*latency-sensitive or latency-insensitive*") [col 5, L3-23] [Fig. 2B].

It would thus be obvious to one of ordinary skill in the art at the time of the invention to combine and/or modify Johnson's invention with additional feature of determining the characteristics of the fragment of electronic data; and moderating one or more interrupts to a processor if the characteristics of the fragment of electronic data indicate that the fragment of electronic data is latency-sensitive data, as disclosed by Duda, for the motivation of advantageously scheduling a resource between elements to maintain a fair long-term allocation of the resource to elements while still satisfying the responsive needs of latency-sensitive elements and to improve device performance [co 2, L29-40].

Claims 11, 20, and 29 state the same limitations as Claim 1 above, and are rejected for the same reasons as they differ only by their statutory category.

As per claim 3, Johnson dislcoses the apparatus of claim 1, wherein said I/O device comprises a network interface card **(NIC) 210** [Col 2, lines 13-26; Col 3, lines 15-32; Figure 2 and 3].

As per claim 5, Johnson discloses the apparatus of claim 1, wherein said I/O device is configured to moderate by substantially immediately asserting said one or more

interrupts of said associated computing platform processor [Col 2, lines 48-51 & Col 7, lines 52-56].

Claims 2, 4, 12, 13, 21, 22, 30, 31 are rejected under 35 U.S.C 103(a) as being unpatentable over Johnson in view of Duda and in further view of Drottar et al (hereinafter Drottar), Patent Number 6,333,929.

As per claim 2, 12, 21 and 31, Johnson in view of Duda and in further view of Drottar discloses the apparatus of claim 1, wherein the latency-sensitive data comprises an acknowledgement (ACK).

Johnson teaches in his invention that data is typically transferred across network segments in the form of packets or frames. Further, the data transferred and written into the buffer of an I/O device, such as a network interface device (NIC), *are written in blocks of data that are in the form of packets or portions of packets* (fragments) [Col 2, Lines 27-42]. Duda discloses analyzing content of data packets to determine the characteristics of the packet/fragment [col 5, L2-23] [Fig. 2B & 3]. However, the combination of Johnson and Duda does not expressly disclose that the portion of said contents of said fragment of data specifically comprises an acknowledgement (ACK).

Drottar, in his invention for formatting and transmitting network packets over a distributed computer system, discloses a packet format that includes a transaction header **640** and a media access control (MAC) header **650** [Col 3, lines 6-9; also Col 11, lines 16-19; Figure 6]. As can be seen in the format for data packets with a MAC

header, the header format includes a field for an ACK/NAK identification and processing [Col 13, lines 1-7; also see Col 10, lines 59-67].

It would therefore be obvious to one ordinarily skilled in the art at the time of the invention to include the packet formatting features employed by Drottar's invention into the combined invention of Johnson and Duda for the motivation of improving packet switching speed and processing efficiency in the transmission of data [Col 16, lines 1-12].

Claims 12 and 21 state the same limitations as Claim 2 above, and are rejected for the same reasons as they differ only by their statutory category.

As per claims 4, 13, and 22, Johnson in view of Drottar discloses the apparatus of claim 1, wherein the latency-sensitive data comprises one or more data packets that have a priority designation [Drottar, Col 2, lines 31-33; also Col 16, lines 1-12 & 25-39].

Johnson teaches in his invention that data is typically transferred across network segments in the form of packets or frames. Further, the data transferred and written into the buffer of an I/O device, such as a network interface device (NIC), *are written in blocks of data that are in the form of packets or portions of packets* (fragments) [Col 2, Lines 27-42]. Duda discloses analyzing content of data packets to determine the characteristics of the packet/fragment [col 5, L2-23] [Fig. 2B & 3]. However, the

combination of Johnson and Duda does not expressly disclose that the portion of said contents of said fragment of data specifically comprises an acknowledgement (ACK).

Drottar, in his invention for formatting and transmitting network packets over a distributed computer system, discloses a packet format that includes a transaction header **640** and a media access control (MAC) header **650** [Col 3, lines 6-9; also Col 11, lines 16-19; Figure 6]. Drottar expressly teaches that the packet headers (MAC Header_650) are comprising *a priority field*, a version field and an address field [Drottar, Col 2, lines 31-33; also Col 16, lines 1-12 & 25-39].

It would therefore be obvious to one ordinarily skilled in the art at the time of the invention to include the packet formatting feature of a field designating prioritization of packets transmitted or received, as disclosed by Drottar, the combined invention of Johnson and Duda for the motivation of improving packet switching speed and processing efficiency in the transmission of data [Col 16, lines 1-12].

Claims 13 and 22 state the same limitations as Claim 4 above, and are rejected for the same reasons as they differ only by their statutory category.

Claims 6-10, 15-19, 24-28 are rejected under 35 U.S.C 103(a) as being unpatentable over Johnson in view of Duda and in further view of Gentry Jr., Patent Number 6,434,651.

As per claim 6, Johnson in view of Duda and in further view of Gentry discloses the apparatus of claim 1, wherein said I/O device is configured to moderate by deferring said one or more interrupts of said associated computing platform processor so that a predetermined number of interrupts per unit of time is not exceeded.

For his invention, Johnson discloses a computer system that includes a host processor, memory, an interface bus and a network interface device (NIC) for communicating with a network [Col 3, lines 16-20]. The NIC informs the host processor that a block of data was received and tha a DMA transfer of data has been performed into the computer memory, via an interrupt [Col 2, Lines 40-51]. Duda discloses analyzing content of data packets to determine the characteristics of the packet/fragment [col 5, L2-23] [Fig. 2B & 3]. However, the combination of Johnson and Duda does not expressly disclose that the network interface device is configured to moderate by deferring one or more interrupts of the host processor so that a predetermined number of interrupts per unit of time is not exceeded.

Gentry, Jr., in his invention for modulating or suppressing the issuance of interrupts from a communication device such as a NIC [Col 1, lines 6-10], discloses an apparatus whereby interrupts normally generated when packets are received by a NIC and transferred to a host processor are alternatingly enabled and disabled. In particular, after one interrupt is issued to and serviced by a host processor, another interrupt in not generated until a *predetermined period of time* has passed for a

specified amount of network traffic has been sent to the host computer system. [Gentry Jr., Col 7, lines 37-47 & 51-56; also Col 8, lines 1-11 & 39-67]

It would therefore be obvious to one ordinarily skilled in the art at the time of the invention to incorporate the interrupt suppression features in Gentry Jr.'s invention into the combined invention of Johnson and Duda so that a host processor can be more responsive to other tasks (e.g. user activity) and to decrease the amount of processor time used to process network traffic, by modulating the number of network interrupts generated by a network interface.

As per claims 7, 16, 25 and 30, Johnson in view of Duda and in further view of Gentry discloses states the apparatus of claim 1, wherein said I/O device is configured to moderate by deferring said one or more interrupts until a particular number of fragments of electronic data of a particular type are received by said I/O device [Gentry Jr., Col 7, lines 19-36, 47-56, & 63-67; Col 8, lines 1-11 and 39-67].

For his invention, Johnson discloses a computer system that includes a host processor, memory, an interface bus and a network interface device (NIC) for communicating with a network [Col 3, lines 16-20]. The NIC informs the host processor that a block of data was received and tha a DMA transfer of data has been performed into the computer memory, via an interrupt [Col 2, Lines 40-51]. Duda discloses analyzing content of data packets to determine the characteristics of the packet/fragment [col 5, L2-23] [Fig. 2B & 3]. However, the combination of Johnson and

Duda does not expressly disclose the apparatus wherein said I/O device is configured to moderate by deferring said one or more interrupts until a particular number of fragments of electronic data of a particular type are received by said I/O device.

Gentry, Jr., in his invention for modulating or suppressing the issuance of interrupts from a communication device such as a NIC [Col 1, lines 6-10], discloses an apparatus whereby interrupts normally generated when packets are received by a NIC and transferred to a host processor are alternatingly enabled and disabled. In particular, Gentry discloses the apparatus wherein said I/O device is configured to moderate by deferring said one or more interrupts until a particular number of fragments of electronic data of a particular type are received by said I/O device [Gentry Jr., Col 7, lines 29-36].

It would therefore be obvious to one ordinarily skilled in the art at the time of the invention to incorporate the feature of the apparatus wherein said I/O device is configured to moderate by deferring said one or more interrupts until a particular number of fragments of electronic data of a particular type are received by said I/O in Gentry Jr.'s invention into the combined invention of Johnson and Duda so that a host processor can be more responsive to other tasks (e.g. user activity) and to decrease the amount of processor time used to process network traffic, by modulating the number of network interrupts generated by a network interface device [Gentry Jr., Col 7, lines 29-36].

Claims 16, 25 and 30 state the same limitations as Claim 1 above, and are rejected for the same reasons as they differ only by their statutory category.

As per claim 8, 17, and 26, Johnson in view of Duda and in further view of Gentry discloses the apparatus of claim 1, wherein said I/O device is configured to moderate by deferring said one or more interrupts until a particular quantity of electronic data is received [Gentry Jr., Col 7, lines 47-56, & 63-67; Col 8, lines 1-11].

For his invention, Johnson discloses a computer system that includes a host processor, memory, an interface bus and a network interface device (NIC) for communicating with a network [Col 3, lines 16-20]. The NIC informs the host processor that a block of data was received and tha a DMA transfer of data has been performed into the computer memory, via an interrupt [Col 2, Lines 40-51]. Duda discloses analyzing content of data packets to determine the characteristics of the packet/fragment [col 5, L2-23] [Fig. 2B & 3]. However, the combination of Johnson and Duda does not expressly disclose the apparatus wherein said I/O device is configured to moderate by deferring said one or more interrupts until a particular quantity of electronic data is received.

Gentry, Jr., in his invention for modulating or suppressing the issuance of interrupts from a communication device such as a NIC [Col 1, lines 6-10], discloses an apparatus whereby interrupts normally generated when packets are received by a NIC and transferred to a host processor are alternatingly enabled and disabled. In particular, Gentry discloses the apparatus wherein said I/O device is configured to

moderate by deferring said one or more interrupts until a particular quantity of electronic data is received [Gentry Jr., Col 7, lines 47-56, & 63-67; Col 8, lines 1-11].

It would therefore be obvious to one ordinarily skilled in the art at the time of the invention to incorporate the feature of the apparatus wherein said I/O device is configured to moderate by deferring said one or more interrupts until a particular quantity of electronic data is received in Gentry Jr.'s invention into the combined invention of Johnson and Duda so that a host processor can be more responsive to other tasks (e.g. user activity) and to decrease the amount of processor time used to process network traffic, by modulating the number of network interrupts generated by a network interface device [Gentry Jr., Col 7, lines 29-36].

Claims 17 and 26 state the same limitations as Claim 1 above, and are rejected for the same reasons as they differ only by their statutory category.

As per claim 9, 18, and 27, Johnson in view of Duda and in further view of Gentry discloses the apparatus of claim 1, wherein said moderation of associated computing platform interrupt scheme is configurable through a user interface.

For his invention, Johnson discloses a computer system that includes a host processor, memory, an interface bus and a network interface device (NIC) for communicating with a network [Col 3, lines 16-20]. The NIC informs the host processor

that a block of data was received and tha a DMA transfer of data has been performed into the computer memory, via an interrupt [Col 2, Lines 40-51]. Duda discloses analyzing content of data packets to determine the characteristics of the packet/fragment [col 5, L2-23] [Fig. 2B & 3]. However, the combination of Johnson and Duda does not expressly disclose the apparatus wherein said moderation of associated computing platform interrupt scheme is configurable through a user interface. Gentry, Jr., in his invention for modulating or suppressing the issuance of interrupts from a communication device such as a NIC [Col 1, lines 6-10], discloses an apparatus whereby interrupts normally generated when packets are received by a NIC and transferred to a host processor are alternatingly enabled and disabled. In particular, Gentry discloses the apparatus wherein said moderation of associated computing platform interrupt scheme is configurable through a user interface [Gentry Jr., Col 7, lines 51-56; Col 8, lines 3-11].

It would therefore be obvious to one ordinarily skilled in the art at the time of the invention to incorporate the feature of the apparatus wherein said moderation of associated computing platform interrupt scheme is configurable through a user interface in Gentry Jr.'s invention into the combined invention of Johnson and Duda so that a host processor can be more responsive to other tasks (e.g. user activity) and to decrease the amount of processor time used to process network traffic, by modulating the number of network interrupts generated by a network interface device [Gentry Jr., Col 7, lines 29-36].

Claims 18 and 27 state the same limitations as Claim 1 above, and are rejected for the same reasons as they differ only by their statutory category.

As per claim 10, 19, and 28, Johnson in view of Duda and in further view of Gentry discloses the apparatus of claim 1, and further comprising: said I/O device further being operative to measure a particular period of time after the receipt of a fragment of electronic data, and further being operative to moderate one or more interrupts of an associated computing platform after said particular period of time has elapsed.

For his invention, Johnson discloses a computer system that includes a host processor, memory, an interface bus and a network interface device (NIC) for communicating with a network [Col 3, lines 16-20]. The NIC informs the host processor that a block of data was received and tha a DMA transfer of data has been performed into the computer memory, via an interrupt [Col 2, Lines 40-51]. Duda discloses analyzing content of data packets to determine the characteristics of the packet/fragment [col 5, L2-23] [Fig. 2B & 3]. However, the combination of Johnson and Duda does not expressly disclose the apparatus further comprising: said I/O device further being operative to measure a particular period of time after the receipt of a fragment of electronic data, and further being operative to moderate one or more interrupts of an associated computing platform after said particular period of time has elapsed.

Gentry, Jr., in his invention for modulating or suppressing the issuance of interrupts from a communication device such as a NIC [Col 1, lines 6-10], discloses an apparatus whereby interrupts normally generated when packets are received by a NIC and transferred to a host processor are alternatingly enabled and disabled. In particular, Gentry discloses the apparatus further comprising: said I/O device further being operative to measure a particular period of time after the receipt of a fragment of electronic data, and further being operative to moderate one or more interrupts of an associated computing platform after said particular period of time has elapsed [Gentry Jr., Col 7, lines 37-47 & 51-56; also Col 8, lines 39-67].

It would therefore be obvious to one ordinarily skilled in the art at the time of the invention to incorporate the feature of the apparatus further comprising: said I/O device further being operative to measure a particular period of time after the receipt of a fragment of electronic data, and further being operative to moderate one or more interrupts of an associated computing platform after said particular period of time has elapsed, as in Gentry Jr.'s invention, into the combined invention of Johnson and Duda so that a host processor can be more responsive to other tasks (e.g. user activity) and to decrease the amount of processor time used to process network traffic, by modulating the number of network interrupts generated by a network interface device [Gentry Jr., Col 7, lines 29-36].

Claims 19 and 28 state the same limitations as Claim 1 above, and are rejected for the same reasons as they differ only by their statutory category.

As per claim 15, Johnson in view of Duda and in further view of Gentry discloses the method of claim 11, wherein said moderating comprises deferring said one or more interrupts of said associated computing platform processor if a predetermined number of interrupts per unit time is met or exceeded

For his invention, Johnson discloses a computer system that includes a host processor, memory, an interface bus and a network interface device (NIC) for communicating with a network [Col 3, lines 16-20]. The NIC informs the host processor that a block of data was received and tha a DMA transfer of data has been performed into the computer memory, via an interrupt [Col 2, Lines 40-51]. Duda discloses analyzing content of data packets to determine the characteristics of the packet/fragment [col 5, L2-23] [Fig. 2B & 3]. However, the combination of Johnson and Duda does not expressly disclose the method wherein said moderating comprises deferring said one or more interrupts of said associated computing platform processor if a predetermined number of interrupts per unit time is met or exceeded.
Gentry, Jr., in his invention for modulating or suppressing the issuance of interrupts from a communication device such as a NIC [Col 1, lines 6-10], discloses an apparatus whereby interrupts normally generated when packets are received by a NIC and transferred to a host processor are alternatingly enabled and disabled. In particular, Gentry discloses the method wherein said moderating comprises deferring said one or more interrupts of said associated computing platform processor if a predetermined

number of interrupts per unit time is met or exceeded [Gentry Jr., Col 7, lines 37-47 & 51-56; also Col 8, lines 39-67].

It would therefore be obvious to one ordinarily skilled in the art at the time of the invention to incorporate the feature of the method wherein said moderating comprises deferring said one or more interrupts of said associated computing platform processor if a predetermined number of interrupts per unit time is met or exceeded, as in Gentry Jr.'s invention, into the combined invention of Johnson and Duda so that a host processor can be more responsive to other tasks (e.g. user activity) and to decrease the amount of processor time used to process network traffic, by modulating the number of network interrupts generated by a network interface device [Gentry Jr., Col 7, lines 29-36].

As per claim 24, Johnson in view of Duda and in further view of Gentry discloses the article of claim 20, wherein said moderating comprises deferring said interrupting of said associated computing platform processor.

For his invention, Johnson discloses a computer system that includes a host processor, memory, an interface bus and a network interface device (NIC) for communicating with a network [Col 3, lines 16-20]. The NIC informs the host processor that a block of data was received and tha a DMA transfer of data has been performed into the computer memory, via an interrupt [Col 2, Lines 40-51]. Duda discloses analyzing content of data packets to determine the characteristics of the

packet/fragment [col 5, L2-23] [Fig. 2B & 3]. However, the combination of Johnson and Duda does not expressly disclose the article wherein said moderating comprises deferring said interrupting of said associated computing platform processor.

Gentry, Jr., in his invention for modulating or suppressing the issuance of interrupts from a communication device such as a NIC [Col 1, lines 6-10], discloses an apparatus whereby interrupts normally generated when packets are received by a NIC and transferred to a host processor are alternatingly enabled and disabled. In particular, Gentry discloses the article wherein said moderating comprises deferring said interrupting of said associated computing platform processor [Gentry Jr., Col 1, Lines 5-10; Figure 1; also Col 7, lines 10-18].

It would therefore be obvious to one ordinarily skilled in the art at the time of the invention to incorporate the feature of the article wherein said moderating comprises deferring said interrupting of said associated computing platform processor, as in Gentry Jr.'s invention, into the combined invention of Johnson and Duda so that a host processor can be more responsive to other tasks (e.g. user activity) and to decrease the amount of processor time used to process network traffic, by modulating the number of network interrupts generated by a network interface device [Gentry Jr., Col 7, lines 29-36].

(10) Response to Argument

Claims 1, 3, 5, 11, 20 and 29

With regards to the claims, and claim 1 in particular, , Applicant argues that the Johnson and Duda prior art references, either individually or in combination, does not teach nor disclose recited features of claim 1, which recites in part:

"moderate one or more interrupts to a processor if the characteristics of the fragment of electronic data indicate that the fragment of electronic data is latency sensitive data."

The Office respectfully disagrees and submits that Applicant has misinterpreted and/or not fully considered all the teachings and disclosures of the Johnson and/or Duda prior art references.

In support of his argument, Applicant specifically argues that "while Johnson discloses the I/O device (NIC) that is directed to improving data transfer latency, he does not teach '*using interrupts*' in any way to achieve this objective." Applicant also remarks that neither Johnson nor Duda teaches "moderating interrupts to a processor based on the characterization that received data fragments (packets) are *latency sensitive*. The Office respectfully disagrees and submits that the recited features of

claim 1 are in fact disclosed by Johnson and/or Duda in accordance with the current requirements and language of the claim recitation.

In response to the argument that "while Johnson discloses the I/O device (NIC) that is directed to improving data transfer latency, he does not teach '*using interrupts*' in any way to achieve this objective", the Office firstly remarks and notes that Johnson expressly discloses the use and/or employment of *interrupts* (i.e., 'notifications' / 'interrupts' to the processors of data transfers and/or requests for data transfers) for exemplary prior art embodiments that utilize a memory-mapped system or, alternatively, DMA systems. For example, Johnson teaches that in the case of a 'memory-mapped system' embodiment, the NIC informed the host processor, *usually by interrupt*, and the host processor controlled the transfer of the data from the buffer to the computer memory" [col 2, L26-51]. Alternatively, and specifically with regards to the embodiment of 'DMA capable systems', Johnson expressly teaches that "additional delays were necessary to configure a bus master device to perform the DMA transfer and to subsequently 'inform' the host processor that the transfer was completed (e.g., by 'interrupt') [col 2, L55-59]. And in an even further alternative, in accordance with his invention, Johnson expressly discloses that 'advanced notification' to the host processor (by way of 'interrupts' generated by the NIC of Johnson's invention) that data has been received from the network and is loaded into host memory is desirable and leads to overall reduction in latency when transferring data from a network to a computer system

[col 3, L9-13] [col 4, L1-31] (e.g., 'the registers 310 enable passing of *interrupt signals* and status signals between the NIC 210 and the computer system 102") [col 6, L36-61].

Johnson's disclosed invention improves upon the 'data latency' (delay) of prior art schemes, such as traditional direct memory access (DMA) or memory-mapped systems, which introduces latency or 'delays' (1) as a result of the system "having to wait until for an entire block of packet data to be written into the buffer of a I/O device (NIC) first, for temporary storage, before being transferred to the main memory of a computer; and/or (2) by 'informing' or providing 'notification' to the host processor (via *interrupts*) of the need to perform a 'transfer' of the buffered data after the full block of data has been received / buffered {in the case of 'memory-mapped' systems} or to 'inform' (*interrupt*) the host processor that the transfer had been completed {in the case of DMA-capable systems} [col 2, L26-65].

Regarding the 'DMA capable systems', Johnson expressly teaches, for example:

"FIG. 5A is a timing diagram illustrating one prior art scheme for transferring blocks of data, where the bus interface device 304 is configured to perform DMA transfers. Each block of data for each packet from the segment 106 is written into a corresponding block of memory in the buffer 302 beginning at a time T0 and ending at a time T2 upon assertion of either the EOB signal or the EOF signal to the processor 306. At time T4 after some delay D1, the processor 306 is *notified* that a new block resides in the buffer 302 for transfer to main memory 204. Such "notification" is typically in the form of an "interrupt". The processor 306 respondingly executes an appropriate interrupt routine or the like to set up the bus interface device 304 to initiate a DMA transfer of the current data block. The bus interface device 304 respondingly initiates the DMA transfer at

time T6 after another delay D2. The DMA transfer is completed at time T8, and the host processor 200 is subsequently notified of the transfer at time T10 after another delay D3. 'Notification' of the host processor 200 is handled by "***asserting an interrupt signal***" or executing a cycle on the I/O bus 206, which signal or cycle is transferred to the host processor 200 by the bus controller 208 or other logic.

Some delay or latency in the process described in FIG. 5A may be reduced if the driver routine has full control of the hardware. In particular, the delay D1 between times T2 and T4 may be reduced or eliminated by 'notifying' the local processor 306 *sooner*, even before the completed transfer of the block to the buffer 302. The processor 306 may respondingly perform setup procedures for the DMA early, so that the DMA transfer by the bus interface device 304 may also be initiated earlier."

[Johnson: col 6, L65 - col 7, L27]

Regarding memory-mapped systems, Johnson expressly teaches for example:

"FIG. 5B is a timing diagram illustrating another prior art scheme for transferring blocks of data, where the bus interface device304 is configured as a bus slave rather than being capable of performing DMA transfers. In this memory-mapped configuration, each block of data for each packet from the segment 106 is stored in the buffer 302 beginning at a time T20 and ending at a time T22 upon assertion of either the EOB or EOF signals. The time from T20 to T22 is about the same as the time from T0 to T2 for same-sized blocks. At time T24 after a delay D4, the host processor 200 is *notified* that a new block resides in the buffer 302 to be transferred to main memory 204. As before, "notification" of the host processor 200 is handled by '***asserting an interrupt signal***' or by executing a cycle on the I/O bus 206, which signal or cycle is transferred to the host processor 200 by the bus controller 208 or other logic. The host processor 200 respondingly begins executing a routine to transfer the data, which begins at a time T26 after another delay D5. This data transfer performed by the host processor 200 is completed at a time T28.

Since the host processor 200 performed the transfer in the memory-mapped scheme, it need not be further notified, thereby 'eliminating one delay D3' (delay resulting from 'interrupt' informing host processor that data transfer or block data has been completed) required in the DMA transfer."

[Johnson: col 7, L40-64]

Additionally, with regards to Johnson's present invention, Johnson expressly teaches:

"The transfer of data from the buffer 302 as indicated in step 610 of FIG. 6 begins before the EOB or EOF signal is asserted if the data value read in step 602 is not the same as the unique value. Thus, data transfer begins while the block is still being written by the net interface logic 300. In this manner, data transfer latency from the network 104 to the computer system 102 is substantially reduced. FIG. 8 is a timing diagram illustrating a system according to the present invention for transferring blocks of data from the buffer 302 to the main memory 204. Again, each block of data for each packet from the segment 106 is stored in the buffer 302 beginning at a time T30 and ending at a time T36 upon assertion of either the EOB or EOF signals. However, at a time T32, prior to time T36, the processor 306 detects that the unique value in the buffer 302 has been overwritten by the new block from the network 104. The processor 306 respondingly prepares the hardware to initiate transfer of the data. At time T34 after a slight delay, still before time T36, data transfer of the current block from the buffer 302 to the main memory 204 is initiated. The transfer to the main memory 204 completes at time T38, and the host processor 200 is 'notified' (i.e, 'by interrupt')at time T40, if necessary. Again, in memory-mapped configurations, the host processor 200 controls the transfer to the main memory 204 and *need not be* subsequently "notified".

Comparison of FIGS. 5A and 5B with FIG. 8 reveals that the transfer of each block of data from the network 104 to the main memory 204 of the computer system 102 completes much faster with the present invention than schemes according to prior art."

[Johnson: col 9, L56 - col 10, L19]

Based on the above disclosures, it is clear that in all three exemplary embodiments, Johnson expressly discloses the recited features of an apparatus such as a I/O device that receives packet / 'packet portions' of data ('fragments of electronic data'), as well as the recited / argued feature of "moderating interrupts" (i.e., asserting or deferring an interrupt signal) to process data packets received and temporarily stored in a buffer of a NIC device. This is especially clear in light of Applicant's own description / definition for the recited feature of "moderating interrupts" [0016]. As defined by Applicant himself, Applicant states:

"*As is well known*, computing platforms *typically* utilize '***interrupts***' to shift control or partially shift control of a processor, and may shift which task is being processed by a processor, or alter the manner in which a task is processed. For example, an 'interrupt' may be asserted in order to stop or slow down the processing of a particular task, and allow it to at least partially process another task, such as, for example, processing data that has been received by an I/O device….Typically, data processing rates may be affected by the number and frequency of interrupts used on a processor, as typically, 'asserting' interrupts will stop the processing of certain functions, and start the processing of other functions. Computing platforms may have one or more 'interrupt schemes'. An 'interrupt scheme', in this context refers to a method, plan, or criteria for 'when' and 'how' to assert or allow the assertion of interrupts. '***Interrupt Moderation***', in this context refers to the 'assertion' or 'deferral' of interrupts based in part on a particular interrupt scheme. For example, an interrupt scheme may be designed to assert or allow the assertion of one or more interrupts of a computing system

processor if a particular device requests that data to be processed, such as for example, an I/O device requesting that a computing system processor process data that the I/O device has received…
……An interrupt scheme may be based on or more factors that may include, for example, asserting one or more interrupts to process data received by an I/O device as quickly as practical or to assert one or more interrupts based on importance of the time sensitivity of the data which is requested to be processed…"

[Application Specification: 0016]

Based on the above meaning of an 'interrupt scheme' and definition for "interrupt moderation" / "moderating one or more interrupts", as provided by Applicant himself, it is evident that Johnson's disclosed prior art embodiments and present invention embodiment properly and clearly satisfy the given definition for the feature. With reference to the embodiments disclosed by Johnson, Johnson expressly discloses "notifying a processor by interrupts" as well as "asserting one or more interrupts" to the processor in order to improve the processing of the data received by the I/O device of his invention, which is in accordance with Applicant's own definition for "interrupt moderation" and "interrupt scheme" above [0016]. Thus, contrary to Applicant's remarks, Johnson -- at the very least -- expressly discloses the argued feature of "moderating one or more interrupts" as defined and described by the written description of the claimed invention.

Further, and with regards to the added limitation of moderating one or more interrupts "if the characteristics of the fragment of electronic data indicate that the fragment of electronic data is latency sensitive data", the Office asserts that this is expressly disclosed by Duda in a related endeavor, as cited by the Office Action.

In this regard, the Office asserts that while Johnson expressly employs and /or 'asserts interrupts' in order to notify the computer processor that data is ready to be transferred, or that transfer of a data block to memory has been 'completed', and also seeks to improve overall latency of the system in processing received data by providing 'advanced notification' (i.e., interrupt) to the processor that 'new data' has been received, he does not expressly disclose that the received packet fragments are 'analyzed' to determine if they have any 'latency-sensitive' characteristics. However, the argued limitation of "determining whether characteristics of the fragments of electronic data are *latency-sensitive*" by an apparatus that employs or works in concert with 'interrupts' *is* expressly disclosed by Duda.

Duda discloses as his invention a *Scheduling Algorithm* that fairly allocates a resource (e.g., CPU control / utilization) to a number of schedulable elements of which some are *latency-sensitive* (e.g., Video packets/frames) [col 1, L65-67]. "The invention enforces long-term fairness to each element while allowing '*latency-sensitive elements*' to be preferably selected (over non-latency sensitive elements / packets)" [Abstract] [col

1, L65 – col 2, L467] [Figs. 1, 2a-b, 3]. For example, and with reference to Figures 2a-b and Figure 3, Duda expressly discloses "moderating interrupts to a processor *based on the characterization that received data fragments are 'latency sensitive*".

Duda expressly discloses that Data Switch 200 *examines* the contents of the data packet and determines the 'service requirements' and destination output port or ports required by the packet. The data packet is then queued into one of the queues that feed the specified output port, and 'queue selection' is based on the data packet's 'service requirements' (for example, latency sensitive data packets can be placed in a different queue than latency insensitive packets, or multicast packets).

Significantly, Duda additionally discloses the implementation of a *Preemptive Scheduling Process* that is used to schedule a resource among a plurality of elements, and which is *"interrupt driven"*. Duda also teaches that the preemptive scheduling algorithm can be performed / implemented by a *computer* executing procedures, as well as by other 'mechanisms' (I/O devices), such as a *Data Switch 200*, which can also effectuate *Preemptive Scheduling Process 300* [col 5, L3 – col 6, L26]. In the computer context (initiated from within the processor), 'system timer interrupts' are initiated; in the data switch context, the *preemptive scheduling process* 300 is "*interrupt driven*" and employs *timer interrupts* as well as *enter timing interrupt, prior art interrupt, and return*

from interrupt procedures to allow an element to have exclusive access to the resource from some number of clock ticks {emphasis added} [col, 6, L-27].

Further, and with reference to Figures 7, 10 and 11, Duda additionally teaches 'updating virtual time' that can be invoked when the 'condition' blocking the execution of a thread is satisfied (e.g., *device interrupt*, or some other condition or exception). Referencing Figure 10, Duda discloses *virtual time borrowing process 1000* that is prefatory to executing *latency-senstive code*. [col 12, L28-26]. The argued limitation of "moderating interrupts to a processor *based on the characterization that received data fragments are 'latency sensitive*" is thus expressly disclosed by Duda.

Given the above reasoning and justifications, it is clear from the teachings and disclosures of the prior art references that the combination of Johnson and Duda teaches all the required features of claim 1, as recited by the claim. Accoridngly, the rejection of claim 1 is maintained by the Office.

Secondly, with regards to the claims, Applicant argues that Johnson 'teaches away' from being modified by Duda in order to arrive at the claimed invention. In support of his argument, Applicant remarks that Johnson discloses the prior art embodiments of 'memory-mapped systems' and 'DMA capable systems' which have their own specific delay or latency 'inefficiencies'. As such, Applicant argues that

Johnson 'counsels against' using interrupts to involve the processor in servicing a NIC data transfer data task. The Office respectfully disagrees and respectfully submits that the disclosures of Johnson and Duda make it clear that both Johnson and Duda are, in fact, related endeavors that seek to reduce the 'latency' of their respective system in the processing of data received by a NIC device. Moreover, the Office remarks that Applicant's comment that "Johnson counsels against using interrupts.." – whether actually accurate or not – has no bearing on the fact that Johnson expressly discloses the recited features of an apparatus comprising an I/O device (NIC) that receives and processes data fragments (packets / packet portions) expressly through the employ of 'interrupts'.

In Johnson, "data transfer latency from a network to a computer system is 'reduced' by an appreciable amount via 'advanced notification' (via interrupt) to the host processor that 'new' data has been received and/or loaded into host memory [Johnson: col 4, L13-31]. Duda provides a 'scheduling mechanism' that fairly allocates over the long-term a 'resource' (e.g., CPU processing time) for processing lower-priority elements (packets) "while still satisfying the responsive needs of *latency-sensitive elements*" (packets) that have higher or 'prioritized' service requirements [Duda: col 2, L25-40 & L58-60] [col 13, L15-26].

Further, the Office remarks that not only is Applicant's argument that "Johnson counsels against using interrupts" nothing more than mere allegation of such a position,

the Office also strongly asserts that Johnson, in fact, provides the basis for further modification by Duda: further reducing 'latency' and optimizing efficiency of an apparatus in processing of received packets fragments / packet portions (i.e., data transfer), and that at least this is obvious to one of ordinary skill in the art. The Office also asserts that it is also obvious to one of ordinary skill that the 'interrupts' that drive the implementation of an 'interrupt-driven' Preemptive Scheduling Process / Mechanism of Duda's invention may be *easily* generated by an 'interrupt apparatus', such as that of Johnson's disclosed invention, which reduces overall latency of a system through optimized /efficient use of interrupts (e.g., providing 'advanced notification' to the host processor by 'interrupt') – and with added consideration to received data fragments (packets / packet portions) that are 'latency-sensitive', as determined by the apparatus of Duda's invention – to arrive at the claimed invention.

In this regard, the Office also reminds Applicant that in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Claims 2, 4, 6-10, 12-13, 15-19, 21-22, 24-28

Lastly, with respect to claims 2, 4, 6-10, 12-13, 15-19, 21-22, 24-28 and 30-31, Applicant argues as to patentability of the claims based on its arguments above for claim 1, as well as the same argument for why Johnson and Duda cannot be combined to teach the claimed invention. However, it has been demonstrated above that the combination of Johnson and Duda teaches all of the recited features of the argued claim(s), and that the modification of Johnson by Duda is proper. The rejection of the above claims are thus maintained by the Office for at least the same reasons provided above for representative claim 1.

In summary, since it has also been shown that all of the limitations of the argued claims are taught and/or disclosed by the combination of the Johnson and Duda prior art references, the Office asserts that the claims are unpatentable, and accordingly maintains its rejection of the claims in view of the applied prior art references.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

(12) Conclusion

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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April 24, 2009
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